REMARKS

Reconsideration of the application is requested.

Applicants acknowledge the Examiner's confirmation of receipt of applicants' certified copies of the priority documents for the German Patent Application 100 61 528.7, filed December 11, 2000 supporting the claim for priority under 35 U.S.C. § 119.

Claims 1-14 are in the application.

In item 2 on page 2 of the above-identified Office Action, claims 1, 3-4, 6-9, 10, and 13-14 have been rejected as being fully anticipated by US Patent No. 6,037,632 to Omura, et al. (hereinafter OMURA) under 35 U.S.C. § 102(b).

More specifically, the Office Action asserts that claims 1, 3-4, 9 and 14 are primarily disclosed through FIG. 6, FIG. 8A, and FIG. 8B of OMURA.

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and, therefore, the claims have not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a semiconductor component including:

> a drift zone which has at least two segments, wherein the distance between two adjacent segments is selected such that a punch-through voltage between adjacent segments corresponds at most to a voltage across said drift zone at twice a rated current.

The OMURA reference discloses a MOSFET transistor operating in a "blocking" mode with p-type base layers 18, n-type source layers 19 embodied in the base layers 18, an n-type substrate 11 and an n-type base layer 13 embodied between the substrate 11 and the base layers 18. The n-type base layer 13 or drift zone is weakly n- doped.

Several buried p-type layers 14 and 16 are disposed at a distance to each other in the base layer 13, such that the breakdown voltage between each n-type base layer 13, 15, and 17 is 200V and the overall breakdown voltage is 600V (col. 9, lines 8-16 and col. 10, lines 10-12). Figs. 8A-8F and Fig. 10A help illustrate the desired operation of the transistor

disclosed in OMURA with regards to the segmented breakdown between p-type layers.

More specifically, the aforementioned figures illustrate how the distances between the various p-type layers 18, 16, and 14 are chosen such that the punch-through voltage between each of the p-type layers is approximately 200V. Thus, the distance between "segments" of the "drift zone" in OMURA is not "**chosen such that a punch-through voltage between adjacent segments corresponds at most to a voltage across said drift zone at twice a rated current**" as recited in claim 1 of the instant application, rather the distance is chosen such that the punch-through voltage between each of the p-type layers is approximately 200V. Consequently, the distance between the adjacent segments in OMURA is much greater than in the instant application.

Furthermore, even assuming *arguendo* that the MOSFET transistors described in OMURA do describe segments disposed at a distance from each other such that the punch-through voltage between adjacent segments corresponds to at most a voltage across the drift zone "at twice a rated current" as recited in claim 1, such a device would not be a viable semiconductor component. Specifically, the semiconductor component described in claim 1 must include a drift zone that is chosen so that the punch-through voltage between segments

is at most "twice a rated current", if the punch-through voltage is 200V between the segments as required from the teachings in OMURA (see Figs. 8A-8F, Fig. 10A, col. 9, lines 8-16 and col. 10, lines 10-12), the resulting operational voltage would need to be **at least 100V** at a rated current.

Accordingly, the segments of a device matching the teachings of OMURA would be placed too far apart to be practical as a power semiconductor component. 100V is not a viable operational voltage level across the drift zone for a semiconductor component, such as a MOSFET transistor, operating in the "on" mode. As is known to one of skill in art, the operational voltage over the drift path region of a MOSFET power component functioning in the "on" operational mode traditionally ranges between about 5V and about 10V.

In contrast, the instant application describes a semiconductor device that places at least two segments within the drift zone at distances "chosen such that a punch-through voltage between said adjacent segments corresponds at most to a voltage across said drift zone at twice a rated current." This enables the semiconductor device described in the instant application to exhibit a low turn-on resistance and a high breakdown voltage while dramatically reducing the pinch-off of the conductive channel in the drift zone in the "on" state.

Clearly, OMURA does not show adjacent segments disposed at a distance "**chosen such that a punch-through voltage between said adjacent segments corresponds at most to a voltage across said drift zone at twice a rated current**" as recited in claim 1 of the instant application. Similarly, OMURA does not teach or suggest that the distance between adjacent segments is chosen "such that **a punch-through voltage** between said adjacent segments **corresponds to a voltage across said drift zone between a rated current and two times the rated current**" as recited in claim 14.

In item 4 on page 3 of the Office Action, claims 5 and 11-12 have been rejected as being obvious over OMURA under 35 U.S.C. § 103(a). In addition to the fact that the dependent claims 5, 11, and 12 are believed to be patentable because they all are ultimately dependent on claim 1, claims 11 and 12 are also not believed to be obvious in view of OMURA. This is because OMURA expressly teaches that the thickness, Ws, of layers 13, 15, and 17 is set to 14 μm (col. 9, line 19) not "between 1 and 2 μm" as recited in claim 11 or "between 0.5 and 1.5 μm" as recited in claim 12. This difference in thickness is indicative of the functional and structural difference between OMURA and the instant application. Namely, OMURA is operating in a "blocking" mode in contrast

to the "on" mode used in the invention of the instant application.

In item 5 on page 4 of the Office Action, claim 2 has been rejected as being obvious over OMURA in view of US 2002/0117715 to Oppermann, et al. (hereinafter OPPERMANN) under 35 U.S.C. § 103(a). In addition to the fact that the dependent claim 2 is believed to be patentable over OMURA because it is ultimately dependent on claim 1, OPPERMANN does not teach or suggest that one segment "directly adjoins said channel zone" and should be disposed at a distance "**chosen such that a punch-through voltage between said adjacent segments corresponds at most to a voltage across said drift zone at twice a rated current**" as recited in claims 1 and 2 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 and 14. Claims 1 and 14 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-14 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

Petition for extension is herewith made. The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of $110.00 in accordance with Section 1.17 is enclosed herewith.Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicants

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